UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,032	07/31/2003	Tirdad Sowlati	051933-1090	9657

24504 7590 08/15/2005

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
100 GALLERIA PARKWAY, NW
STE 1750
ATLANTA, GA 30339-5948

EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	**PAPER NUMBER**
2817	

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/632,032	SOWLATI, TIRDAD	
	Examiner	Art Unit	
	michael b. shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 7-22-2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1 and 3-44 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 32-44 is/are allowed.

6)☒ Claim(s) 1,3-17,21-27 and 29-31 is/are rejected.

7)☒ Claim(s) 18-20 and 28 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The indicated allowability of claims 2-4 and 8-31 is withdrawn in view of the newly discovered reference(s) to Cyrusian 6,570,447 (Cyrusian). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-17, 21-27 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art as presented on pages 1-9 of the instant application (AAPA) in view of Cyrusian et al. 6,570,447 (Cyrusian).

AAPA discloses that various conventional variable gain amplifiers can be used in a communications arrangement that employs a source to "derive" the control voltages, in such a variable gain amplifier arrangement that utilizes a degeneration element and a "collector load", though the use of a "differential input control voltage" (See page 9, around line 21). Also note the use of single ended voltage and bandgap voltage, i.e. reference voltage, to derive the differential input control voltage as shown in Figure 1. Figure 1 also shows that a conventional gain amplifier can operate at different frequencies such as base-band and IF. Also note the feedback loop with VGA 110. AAPA (Figure 3) also discloses the use of a resistor arrangement like that of 354 to control a plurality of FET controlled resistors so as to form a variable resistor element.

Figures 8 and 9 and the relevant text of Cyrusian discloses a conventional variable gain amplifier system having a differential pair of transistors 222(Mp) and 232(Mn), a degeneration element Rin(142), a "collector load" Rout(162) of a "similar type" to the degeneration element. As noted in previous office actions "of a similar type" is very broad claim language and there is no specific definition in the specification for this term and thus it is given its usual meaning. It is also noted that there is no specific definition for the term "collector load" in the specification. It is noted that at least claim 1 does not even specify that the degeneration element and the

"collector load" are even transistor elements. They could be two resistors like that of the prior art Figure 1 of Cyrusian. However, the embodiment of Figure 8A of the instant application shows the degeneration element and the collector load being formed from the same conductivity MOSFETs and this is exactly the composition of the degeneration and collector load elements of Cyrusian. Note that MOSFETs NR1 and NR2 are of the same conductivity type. Also note the use of current mirrors CMP and CMN that parallels the use of current mirrors 712 and 714 shown in Figure 8A of the instant application. Figures 8 and 9 of Cyrusian are closer to the actual invention of Applicant than Figure 1 of Cyrusian. Throughout the instant application Applicant attributes the functional language "wherein a gain of the variable gain amplifier is determined by a physical dimension ratio of the collector load to the degeneration element for a differential control voltage equal to zero volts" to the use of the same conductivity type transistors that make up the collector load and the degeneration elements. See the top of page 20 of the instant application: "When control voltages Vc1 and Vc2 are substantially similar in value (e.g. zero volts differential input control voltage), and an emitter degeneration element 708 and collector load 716 comprising of the same type of variable resistance is used, the gain of the IF VGA 650a is substantially constant despite changes in voltage supply...". Therefore for these reasons above Cyrusian inherently provides for the functional language of at least claim 1. As noted above applicant has not specifically defined "a collector load" including to mean that the differential pair of transistors must be composed of bi-polar transistors. Cyrusian uses MOSFETs. However, alternatively, Cyrusian discloses the claimed invention except for the use of bipolars for the differential pair of MOSFETs. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize bi-polar transistors for the differential MOSFET transistors of Cyrusian since the examiner takes Official Notice of the equivalence of bipolars and MOSFETs for their use in the electronic art and the selection of any of these known equivalents to provide a transistor function would be within the level of ordinary skill in the art. Claim 1 has been amended to recite "a first control voltage to vary the resistance of the degeneration element and a second control voltage to vary the resistance of the collector load, wherein the first control voltage and the second control voltage are derived from the differential input control voltage". The two control voltages of Cyrusian clearly controls the varying of resistance of these elements. The Figure 8 embodiment of Cyrusian obtains these control voltages from two feedback arrangements and the Figure 9 embodiment of Cyrusian obtains these control signals from a microprocessor. Both embodiments are silent of the

functional language of "wherein the first control voltage and the second control voltage are derived from the differential input control voltage" and "the differential input control voltage is derived from a single ended voltage and a bandgap voltage". There is no structure that can provide for this functional language. "Apparatus claims must be structurally distinguishable from the prior art" see MPEP 2114.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a variable gain amplifier made obvious above for the variable gain amplifiers (baseband and IF) of the AAPA arrangement because as the AAPA reference discloses the use of multiple conventional variable gain amplifier arrangements that employ a degeneration element and a collector load for the variable gain amplifier elements one of ordinary skill in the art would have been motivated to replace any of the conventional variable gain amplifier arrangements of AAPA with any art recognized equivalent variable gain amplifier such as the variable gain amplifier arrangement made obvious above involving Cyrusian.

Claims like claims 5 and 6 recite a second differential amplifier arrangement having the same structure as that of the first. Claim 5 is clearly met from that above but from claim 6 it appears that these two amplifier arrangements are cascaded, i.e. connected in series, but again claim 6 recites function and no structure to enable that function. However, providing amplifiers in cascade to form a single amplifier unit of higher gain than either one alone is common in the art and is an art recognized equivalent structure to a single amplifier. It would have been obvious to one having ordinary skill in the art at the time the invention was made to replace the single amplifier arrangement made obvious above with two of the same type connected in cascade since the examiner takes Official Notice of the equivalence of a single amplifier and two amplifiers connected in cascade for their use in the electronic art and the selection of any of these known equivalents to provide an amplifier function would be within the level of ordinary skill in the art. One of ordinary skill in the art would have been additionally motivated to make the combination so as to utilize amplifiers with less overall gain. Typically lower gain amplifiers have less noise and are less expensive that a single high gain amplifiers and it is a real advantage known to those of ordinary skill to utilize amplifiers with less noise and less expense in a cascade arrangement.

With respect to claims like claim 15, here the opposite conductivity type transistors are employ over the prior art transistor types. Claim 15 forms the same basic circuit as claim 14 that is obvious as indicted above except that the conductivity types are opposite that of claim

14. However, it is generally known that an art recognized equivalent circuit is formed from transistors of opposite conductivity type than the original circuit. Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to reverse the conductivity of the transistor elements of the prior art as well as apply the appropriate voltage since the examiner takes Official Notice of the equivalence of a circuit formed of having transistors of a certain conductivity type(s) and the same circuit wherein the conductivity types are opposite that of the first in the electronic art and the selection of any of these known equivalents to provide circuit that works on opposite conductivity types yet retain the same basic function of the first circuit would be within the level of ordinary skill in the art.

It also would have been obvious to one having ordinary skill in the art at the time the invention was made to replace the variable resistive elements of the combination made obvious above with one that employs a plurality of MOSFETs and a resistive ladder to selectively turn these MOSFETs on because AAPA (Figure 3) shows the art recognized equivalence of such an arrangement for providing a variable resistance function in an amplifier arrangement that employs a degeneration element and a collector load. One of ordinary skill in the art would have been motivated to replace one variable resistance element with another and specifically with one that is taught and shown by AAPA (Figure 3) given the art recognized equivalents of these resistor arrangements and the selection of any of these known equivalent to provide a variable resistance function would be within the level of ordinary skill in the art.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ruth, Jr. et al. has been cited because it shows that a differential pair of transistors 220 and 222 can be used with current mirrors composed of MOSFETs in "a similar type" of amplifier structure to that claimed and to that of Cyrusian.

Claims 18-20 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

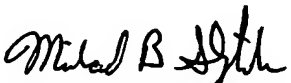
Claims 32-44 are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
August 8, 2005



Michael B Shingleton
Primary Examiner
Group Art Unit 2817